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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/064,474	04/22/98	ROY S	TRA-040

LMC1/0606

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EXAMINER	
WHITMORE, S	
ART UNIT	**PAPER NUMBER**
2783	4

DATE MAILED: 06/06/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/064,474	Subhash et al.
Examiner	**Group Art Unit**
Stacy Whitmore	2783

☒ Responsive to communication(s) filed on *Mar 13, 2000*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-21 and 23-27* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-5, 11-15, 19-21, and 23-27* is/are rejected.

☒ Claim(s) *6-10 and 16-18* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

FINAL ACTION

1. Claims 1-21, and 23-27 are presented for examination.

2. It is noted that the present application does not contain line numbers in the specification of claims, and does not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the Examiner and Applicant all future correspondence should include the recommended numbering.

Claim Rejections - 35 U.S.C. § 112

3. Claims 4, 14, and 23, 26, and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The claim language in the following claims is not clearly understood:

I. As per claims 4, 14, and 23, 26, and 27, it is unclear exactly what is meant by "indication whether or not an instruction has been executed since a previous processor cycle". (Does this mean that information about each instruction is updated when an indication is given that an instruction has or has not been executed or does this mean that the information about each instruction is updated which includes information that an instruction has or has not been executed? explain.)

4. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Segars et al. (6,026,503).

5. As for claim 21, Segars et al. taught a method of debugging a processor, said method comprising:

providing information about processor activity in real time (col. 12, lines 59-67);

associating the instructions executed by the processor with information about processor activity (abstract),wherein

said step of providing information about processor activity includes providing information that the processor has not executed an instruction during the last processor cycle (col. 13, lines 1-47).

6. Claims 1, 2, 5, 11-12, 15, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Folwell et al. (5,473,754) in view of Kaneko (5,440,700).

7. Folwell et al. and Kaneko were cited in a prior office action, dated 11/24/99.

8. As for claim 1, Folwell et al. taught the invention substantially as claimed, including a processor having a real time debugging interface (abstract), comprising:

a) instruction memory means (fig. 2, element 21),

b) program counter means connected to said instructino memory (col. 5, lines 4-5),

c) cause register means for indicating information regarding interrupts and exceptions (col. 5, lines 1-10, and Table 4), and

d) first decoder means for indicating information about an instruction executed by the processor during a clock cycle (fig. 2, element 22),

the first decoder connected to the instruction memory (fig. 1, elements 21-22, and the cause register, where the first decoder has a first output providing information regarding activity of the processor (fig. 2, elements 24 and 26, fig. 4, elements 52, 53, and 54, col. 1, lines 62-67, col. 2, lines 1-4).

Folwell et al. does not specifically teach the first decoder coupled to the program counter. However, Kaneko disclosed the program counter coupled to a decoder (col.4, lines 30-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Folwell et al. and Kaneko because it would allow for a means of maintaining status in the debugging process (see Kaneko, col. 2, lines 27-33).

Folwell et al. does not specifically teach the decoder operating in real time. However, Folwell et al. did disclose the decoder operating directly with instruction flow and the debug port, both of which operate in real time (see abstract, lines 12-19, col. 2, tables 1-3, and col. 4, lines 55-

57). It would have been obvious for one of ordinary skill in the art at the time the invention was made that Folwell et al.'s decoder operates in real time because it is part of normal program operation which operates in real time.

9. As for claim 11, Folwell et al. taught the invention substantially as claimed, including the limitations as cited in claim 1. Folwell et al. Did not specifically disclose plural elements within an embedded system. However, Folwell et al. disclosed his debug device coupled to a host work station via a SCSI bus (fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a plurality of elements in an embedded system into Folwell et al.'s system because Folwell et al.'s system was expandable via the SCSI.

10. As for claims 2, and 12, Folwell et al. taught the information about processor activity includes information as to at least one of a jump instruction has been executed (col. 2 table 3), a jump instruction based on the contents of a register has been executed (col. 2, table 3), a branch has been taken (col. 2, table 2), and an exception has been encountered (col. 5, table 4).

11. As for claims 5 and 15, Folwell et al. did not specifically teach the first output is a three bit parallel output. However, Folwell et al. disclosed a parallel output of more than three bits (fig. 2, elements 24 and 26). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Folwell et al.'s performed the same function as claimed by applicant because Folwell et al.'s parallel output included at least three bits of information and could have been designed to use three bits as an output.

12. As for claims 19, Folwell et al. disclosed the processor is on a chip having a plurality of pins (col. 1 lines 5-9), and the first output and data output are provided via some of the pins (fig. 1, element 25 and fig. 2, element 26).

13. As for claims 20, Folwell et al. disclosed the first output is an n-bit parallel output (fig. 2, element 26), and the data output is a serial output (see as cited in the rejection of claim 15).

14. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Segars et al. (6,052,774) in view of Ueki (5,428,618).

15. Ueki was cited in a prior office action, dated 11/24/99.

16. As for claim 23, Segars et al. taught the invention substantially as claimed , including the method of debugging a processor as cited in the rejection of claim 21.

Segars et al. did not specifically teach said step of providing information about processor activity includes providing information about every instruction executed by the processor.

However, Ueki et al. disclosed providing information about every instruction executed by said processor (see abstract, lines 11-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Folwell et al. and Ueki et al. because Ueki et al.'s activity information would improve the integrity of Folwell et al.'s system to be able to backtrack for recovering an internal state of the system (see Ueki et al., abstract).

17. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Segars et al. (6,052,774) in view of Folwell et al. (5,473,754).

18. As for claims 24 and 25, Segars et al. taught the invention substantially as claimed, including the method of debugging a processor as cited in the rejection of claim 1.

Segars et al. did not specifically teach

[24] the information about processor activity includes information as to at least one of a jump instruction has been executed, a jump instruction based on the contents of a register has been executed, a branch has been taken, and an exception has been encountered,

[25], an indication of an event of a change in status of an interrupt line, internal processor exception, or a jump based on the contents of a register.

Folwell et al. taught [24] the information about processor activity includes information as to at least one of a jump instruction has been executed (col. 2, table 3), a jump instruction based on the contents of a register has been executed (col. 2, table 3), a branch has been taken (col. 2, table 2), and an exception has been encountered (col. 5, table 4), and

[25], an indication of an event of a change in status of an interrupt line, internal processor exception, or a jump based on the contents of a register (col. 1, line 64 - col. 2, line 3, and col. 8, lines 1 - 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Segars et al. and Folwell et al. because having [24] information about processor activity that includes information as to at least one of a jump instruction has been executed, a jump instruction based on the contents of a register has been executed, a branch has been taken, and an exception has been encountered, [25], an indication of an event of a change in status of an interrupt line, internal processor exception, or a jump based on the contents of a register would improve the debugging system of Segars et al. by allowing for the understanding of how program flow discontinuities are handled (Folwell et al., col. 2, lines 22-24).

19. Claims 3 and 13 are viewed as similar to claims 1, 11, and 21, are rejected for the reasons as cited in the rejections of claims 1, 11, and 21.

20. Claims 4, 14, and 26-27 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

21. Claims 6-10, and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. Applicant's arguments with respect to claims 21, and 23-25 filed 9/13/99, have been fully considered but are not deemed to be persuasive and are moot in view of the new grounds of rejection.

23. In the remarks on page 6, applicant argues in substance:

A: That term "connected" has the same meaning as "directly coupled".

Examiner respectfully disagrees with applicant.

As to point A: The term connected does not exclude intermediate elements between coupled elements. (See as cited and defined in Meriam Webster's Collegiate Dictionary, Tenth Ed. dictionary definitions [3]direct, page 328; [1]directly, page 328; and connected, pages 244-245).

24. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CAR 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a final rejection has been discontinued by the Office. See 1021 TMOG 35. A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CAR 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Stacy Whitmore, whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday and alternate Fridays from 6:30AM - 4:00PM. The group fax number is (703) 306-5404.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Meng Ai T. An*, can be reached on *(703) 305-9678.*

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Stacy Whitmore
Jun 2, 2000

John A. Follansbee
Patent Examiner